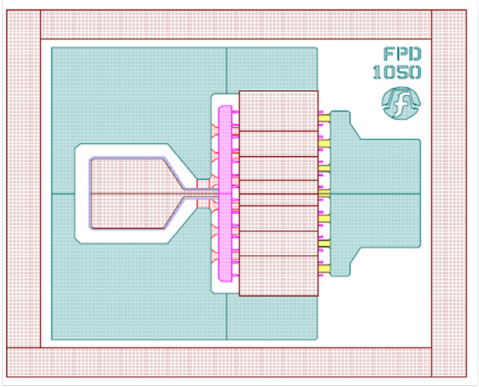
GaAs Devices

0.75 W POWER pHEMT

FPD1050

The FPD1050 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a 0.25 µm x 1050 µm Schottky barrier gate, defined by high resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications.



KEY CHARACTERISTICS

- 28.5 dBm Linear Output Power at 12 GHz
- 11 dB Power Gain at 12 GHz
- 14 dB Max Stable Gain at 12 GHz
- 41 dBm OIP3
- 45 % Power-Added Efficiency

APPLICATIONS

- Narrowband and Broadband High-Performance Amplifiers
- SATCOM Uplink Transmitters
- PCS/Cellular Low-Voltage High-Efficiency Output Amplifiers
- Medium-Haul Digital Radio Transmitters

BARE DIE

0.47 mm x 0.44 mm x 0.075 mm

100% RoHS Compliant

COHERENT

Typical Performance

Parameter	Symbol	Min	TYP	Max	Unit	Conditions	
P_{1dB} Gain Compression	P_{1dB}	27.5	28.5		dBm	V_{DS} = 8 V, I_{DS} = 50 % I_{DSS}	
Maximum Stable Gain (S21/S12)	MSG		14.0		dB	V_{DS} = 8 V, I_{DS} = 50 % I_{DSS},	
Power Gain at P_{1dB}	G_{1dB}	10.0	11.0		dB	V_{DS} = 8 V, I_{DS} = 50 % I_{DSS}	
Power-Added Efficiency	PAE		45		%	V_{DS} = 8 V, I_{DS} = 50 % I_{DSS}, P_{OUT} = P_{1dB}	
Output Third-Order Intercept Point	OIP_3		39		dBm	V_{DS} = 8 V, I_{DS} = 50 % I_{DSS}	Matched for optimal power
			41				Tuned for best IP3
Saturated Drain-Source Current	I_{DSS}	260	325	385	mA	V_{DS} = 1.3 V, V_{GS} = 0 V	
Maximum Drain-Source Current	I_{MAX}		520		mA	V_{DS} = 1.3 V, V_{GS}≈+1 V	
Transconductance	G_M		280		mS	V_{DS} = 1.3 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSO}		15		µA	V_{GS} = -5 V	
Pinch-Off Voltage	V_P		|1.0|		V	V_{DS} = 1.3 V, I_{DS} = 1 mA	
Gate-Source Breakdown Voltage	VBD_{GS}	|12.0|	|14.0|		V	I_{GS} = 3 mA	
Gate-Drain Breakdown Voltage	VBD_{GD}	|14.5|	|16.0|		V	I_{GD} = 3 mA	
Thermal Resistivity (see Note)	θ_{JC}		45		°C/W	V_{DS} > 6 V	

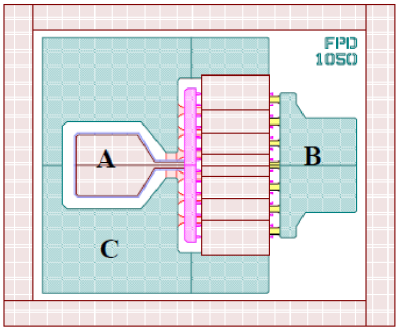
Note: $T_{AMBIENT}$ = 22 °C, RF specifications measured at f=12GHz using CW signal

Absolute Maximum Ratings[1]

Parameter	Symbol	Test Conditions	Absolute Maximum
Drain Source Voltage[2]	V_{DS}	-3 V <V_{GS}<-0.5 V[2]	10 V
Gate-Source Voltage	V_{GS}	0 V < V_{DS} < +8 V	-3 V
Drain Source Current	I_{DS}	For V_{DS} < 2 V	I_{DSS}
Gate Current	I_G	Forward or reverse current	10 mA
RF Input Power	P_{IN}	Under any acceptable bias state	23 dBm
Channel Operating Temperature	T_{CH}	Under any acceptable bias state	175 °C
Storage temperature	T_{STG}	Non-Operating Storage	-65 °C to 150° C
Total Power Dissipation[3, 4, 5]	P_{TOT}	See De-Rating Note below	3.4 W
Simultaneous Combination of Limits[6]		2 or more max. limits	80 %

Notes:
1. $T_{AMBIENT}$=22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
2. Operating at absolute maximum V_D continuously is not recommended. If operation at 10 V is considered then IDS must be reduced in order to keep the part within its thermal power dissipation limits. Therefore V_{GS} is restricted to <-0.5 V.
3. Total Power Dissipation to be de-rated as follows above 22 °C: P_{TOT}=3.4- (0.022 W/°C)xT_{HS}, where T_{HS}=heatsink or ambient emperature above 22 °C. Example: For a 85 °C carrier temperature: P_{TOT}=3.4-(0.022x(85-22))=2.01 W
4. Total Power Dissipation (P_{TOT}) defined as (P_{DC}+P_{IN})–P_{OUT}, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
5. Users should avoid exceeding 80 % of 2 or more Limits simultaneously.
6. Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto an Au-plated copper heatsink or rib.

Die Layout



Pad Layout

Name	Description	PIN Coordinates (µm)
A	Gate Pad	130, 220
B	Drain Pad	380, 220
C	Source Pad	

Note: co-ordinates are referenced from the bottom left hand corner of the die to the centre of the bond pad opening.

Die Size (µm)	Die Thickeness (µm)	MIN. Bond Pad Opening (µm x µm)
470 x 340	75	67 x 77

Caution! ESD sensitive device

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.
RoHS status based on EUDirective2002/95/EC (at time of this document revision).
The information in this publication is believed to be accurate and reliable. However, no responsibility is assumed by II-VI Compound Semiconductors Ltd for its use, nor for any infringement of patents, or other rights of third parties, resulting from its use. No license is granted by implication or otherwise under any patent or patent rights of II-VI Compound Semiconductors Ltd. II-VI Compound Semiconductors Ltd reserves the right to change component circuitry, recommended application circuitry and specifications at any time without prior notice.

Preferred Assembly Instructions

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.
The back of the die is metallized and the recommended mounting method is by the use of conductive epoxy. Epoxy should be applied to the attachment surface uniformly and sparingly to avoid encroachment of epoxy on to the top face of the die and ideally should not exceed half the chip height. For automated dispense Ablestick LMISR4 is recommended. For manual dispense Ablestick 84-1 LMI or 84-1 LMIT are recommended. These should be cured at a temperature of 150°C for one hour in an oven especially set aside for epoxy curing only. If possible, the curing oven should be flushed with dry nitrogen. The gold-tin (80% Au 20% Sn) eutectic die attach has a melting point of approximately 280°C but the absolute temperature being used depends on the leadframe material used and the particular application. The time at maximum temperature should be kept to a minimum.
This part has gold (Au) bond pads requiring the use of gold (99.99% pure) bondwire. It is recommended that 25µm diameter gold wire be used. Recommended lead bond technique is thermocompression wedge bonding with 0.001" (25µm) diameter wire. Bond force, time, stage temperature, and ultrasonics are all critical parameters and the settings are dependent on the setup and application being used. Ultrasonic or thermosonic bonding is not recommended.
Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimized especially when making RF or ground connections.

Handling Precautions
To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL Rating
These devices should be treated as Class 0B (125V to <250V) as defined in JEDEC Standard No. JS-001 and subsequent revisions. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

Reliability
An MTTF in excess of 4 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

Disclaimers
This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information

DELIVERY QUANTITY	DELIVERY QUANTITY
Full Pack (100)	FPD1050 - 100
Small Quantity (25)	FPD1050 - 025
Sample Quantity (3)	FPD1050 - 003

sales@ii-vi.com
www.ii-vi.com