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Application Note AN-2171

100G QSFP28 SWDM EEPROM Application Note Rev A

Introduction

The purpose of this application note is to document the EEPROM contents of Finisar's 100 Gigabit Ethernet QSFP28 SWDM modules. This application note applies to 100GE (4X25G) QSFP28 SWDM Finisar part number FTLC9152RGPL

All registers are supported per SFF-8665 REV 1.9 "QSFP+ 28Gb/s 4X Pluggable Transceiver Solutions (QSFP28)". The EEPROM Mapping below is meant to be an inclusive listing of what is supported by the transceiver.

Applicable Documents, Standards and MSA's

1. SFF-8665 "QSFP+ 28Gb/s 4X Pluggable Transceiver Solutions (QSFP28)", REV 1.9, June 29, 2015 and associated SFF documents:
    a. SFF-8661
    b. SFF-8679
    c. SFF-8636
    d. SFF-8662
    e. SFF-8663
    f. SFF-8672
    g. SFF-8683

2. IEEE802.3bm, CAUI-4 interface

How to use this Application Note

Please refer to the SFF-8665 for information on the available EEPROM memory content, then compare with what is listed below.
Register content specific to FTLC9152RGPL will be marked in parentheses ( ).
The non-used addresses are highlighted in yellow. These are optional per the MSA, thus not required to be implemented.

This application note includes the recommended initialization sequence for the QSFP28 module that is installed into a customer system. Please refer to page 35.

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Content
The following are the EEPROM maps of the QSFP28 transceiver:
Legend:

No highlight = implemented.

Yellow highlight = Optional / not implemented

ADDRESS A0H LOWER PAGE 00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
0	0		RO	Identifier	QSFP28 (SFF-8636)	11
1	1		RO	Revision Compliance	SFF-8636 Rev 2.5	08
2	2	7 ~ 3	RO	RESERVED	Monitor	
		2		Flat_mem: Upper memory flat or paged. Flat memory: 0= paging, 1= Page 00h only		
		1		IntL: Digital state of the IntL Interrupt output pin (if pin supported)		
		0		Data_Not_Ready		
3	3	7	RO	L-TX4 LOS. Latched TX LOS indicator, channel 4	Monitor	
		6		L-TX3 LOS. Latched TX LOS indicator, channel 3		
		5		L-TX2 LOS. Latched TX LOS indicator, channel 2		
		4		L-TX1 LOS. Latched TX LOS indicator, channel 1		
		3		L-RX4 LOS. Latched RX LOS indicator, channel 4		
		2		L-RX4 LOS. Latched RX LOS indicator, channel 3		
		1		L-RX4 LOS. Latched RX LOS indicator, channel 2		
		0		L-RX4 LOS. Latched RX LOS indicator, channel 1		
4	4	7	RO	Latched TX, Adaptive EQ fault indicator, channel 4 (if supported)		
		6		Latched TX, Adaptive EQ fault indicator, channel 3 (if supported)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		5		Latched TX, Adaptive EQ fault indicator, channel 2 (if supported)	Monitor	
		4		Latched TX, Adaptive EQ fault indicator, channel 1 (if supported)		
		3		Latched TX Transmitter/Laser fault indicator, channel 4		
		2		Latched TX Transmitter/Laser fault indicator, channel 3		
		1		Latched TX Transmitter/Laser fault indicator, channel 2		
		0		Latched TX Transmitter/Laser fault indicator, channel 1		
5	5	7	RO	Latched TX CDR LOL indicator, ch 4	Monitor	
		6		Latched TX CDR LOL indicator, ch 3		
		5		Latched TX CDR LOL indicator, ch 2		
		4		Latched TX CDR LOL indicator, ch 1		
		3		Latched RX CDR LOL indicator, ch 4		
		2		Latched RX CDR LOL indicator, ch 3		
		1		Latched RX CDR LOL indicator, ch 2		
		0		Latched RX CDR LOL indicator, ch 1		
6	6	7	RO	Latched high temperature alarm	Monitor	
		6		Latched low temperature alarm		
		5		Latched high temperature warning		
		4		Latched low temperature warning		
		3 ~ 1		Reserved		
		0		Initialization complete flag: This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at byte 6, bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module.	implemented	
7	7	7	RO	Latched high supply voltage alarm	Monitor	
		6		Latched low supply voltage alarm		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		5		Latched high supply voltage warning	Monitor	
		4		Latched low supply voltage warning		
		3 ~ 0		Reserved		
8	8			Vendor Specific		
9	9	7	RO	Latched high RX power alarm, channel 1	Monitor	
		6		Latched low RX power alarm, channel 1		
		5		Latched high RX power warning, channel 1		
		4		Latched low RX power warning, channel 1		
		3		Latched high RX power alarm, channel 2		
		2		Latched low RX power alarm, channel 2		
		1		Latched high RX power warning, channel 2		
		0		Latched low RX power warning, channel 2		
10	0A	7	RO	Latched high RX power alarm, channel 3	Monitor	
		6		Latched low RX power alarm, channel 3		
		5		Latched high RX power warning, channel 3		
		4		Latched low RX power warning, channel 3		
		3		Latched high RX power alarm, channel 4		
		2		Latched low RX power alarm, channel 4		
		1		Latched high RX power warning, channel 4		
		0		Latched low RX power warning, channel 4		
11	0B	7	RO	Latched high TX bias alarm, channel 1	Monitor	
		6		Latched low TX bias alarm, channel 1		
		5		Latched high TX bias warning, channel 1		
		4		Latched low TX bias warning, channel 1		
		3		Latched high TX bias alarm, channel 2		
		2		Latched low TX bias alarm, channel 2		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1		Latched High TX bias warning, channel 2		
		0		Latched low TX bias warning, channel 2		
12	0C	7	RO	Latched high TX bias alarm, channel 3	Monitor	
		6		Latched low TX bias alarm, channel 3		
		5		Latched high TX bias warning, channel 3		
		4		Latched low TX bias warning, channel 3		
		3		Latched high TX bias alarm, channel 4		
		2		Latched low TX bias alarm, Channel 4		
		1		Latched high TX bias warning, channel 4		
		0		Latched low TX bias warning, channel 4		
13	0D	7	RO	Latched high TX Power alarm, channel 1	Monitor	
		6		Latched low TX Power alarm, channel 1		
		5		Latched high TX Power warning, channel 1		
		4		Latched low TX Power warning, channel 1		
		3		Latched high TX Power alarm, channel 2		
		2		Latched low TX Power alarm, channel 2		
		1		Latched High TX Power warning, channel 2		
		0		Latched low TX Power warning, channel 2		
14	0E	7	RO	Latched high TX Power alarm, channel 3	Monitor	
		6		Latched low TX Power alarm, channel 3		
		5		Latched high TX Power warning, channel 3		
		4		Latched low TX Power warning, channel 3		
		3		Latched high TX Power alarm, channel 4		
		2		Latched low TX Power alarm, Channel 4		
		1		Latched high TX Power warning, channel 4		
		0		Latched low TX Power warning, channel 4		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
15	0F		RO	Reserved		
16	10		RO	Reserved		
17	11		RO	Reserved		
18	12		RO	Reserved		
19	13		RO	Vendor Specific		
20	14		RO	Vendor Specific		
21	15		RO	Vendor Specific		
22	16		RO	Internally measured temperature (MSB)		
23	17		RO	Internally measured temperature (LSB)		
24	18		RO	Reserved		
25	19		RO	Reserved		
26	1A		RO	Internally measured supply voltage (MSB)		
27	1B		RO	Internally measured supply voltage (LSB)		
28	1C		RO	Reserved		
29	1D		RO	Reserved		
30	1E		RO	Vendor Specific		
31	1F		RO	Vendor Specific		
32	20		RO	Vendor Specific		
33	21		RO	Vendor Specific		
34	22		RO	Internally measured RX input power, channel 1 (MSB)		
35	23		RO	Internally measured RX input power, channel 1 (LSB)		
36	24		RO	Internally measured RX input power, channel 2 (MSB)		
37	25		RO	Internally measured RX input power, channel 2 (LSB)		
38	26		RO	Internally measured Rx input power, channel 3 (MSB)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
39	27		RO	Internally measured Rx input power, channel 3 (LSB)		
40	28		RO	Internally measured Rx input power, channel 4 (MSB)		
41	29		RO	Internally measured Rx input power, channel 4 (LSB)		
42	2A		RO	Internally measured TX bias, channel 1 (MSB)		
43	2B		RO	Internally measured TX bias, channel 1 (LSB)		
44	2C		RO	Internally measured TX bias, channel 2 (MSB)		
45	2D		RO	Internally measured TX bias, channel 2 (LSB)		
46	2E		RO	Internally measured TX bias, channel 3 (MSB)		
47	2F		RO	Internally measured TX bias, channel 3 (LSB)		
48	30		RO	Internally measured TX bias, channel 4 (MSB)		
49	31		RO	Internally measured TX bias, channel 4 (LSB)		
50	32		RO	Internally measured TX Power, channel 1 (MSB)		
51	33		RO	Internally measured TX Power, channel 1 (LSB)		
52	34		RO	Internally measured TX Power, channel 2 (MSB)		
53	35		RO	Internally measured TX Power, channel 2 (LSB)		
54	36		RO	Internally measured TX Power, channel 3 (MSB)		
55	37		RO	Internally measured TX Power, channel 3 (LSB)		
56	38		RO	Internally measured TX Power, channel 4 (MSB)		
57	39		RO	Internally measured TX Power, channel 4 (LSB)		
58	3A		RO	Reserved Channel Monitor set		
59	3B		RO	Reserved Channel Monitor set		
60	3C		RO	Reserved Channel Monitor set		
61	3D		RO	Reserved Channel Monitor set		
62	3E		RO	Reserved Channel Monitor set		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
63	3F		RO	Reserved Channel Monitor set		
64	40		RO	Reserved Channel Monitor set		
65	41		RO	Reserved Channel Monitor set		
66	42		RO	Reserved Channel Monitor set		
67	43		RO	Reserved Channel Monitor set		
68	44		RO	Reserved Channel Monitor set		
69	45		RO	Reserved Channel Monitor set		
70	46		RO	Reserved Channel Monitor set		
71	47		RO	Reserved Channel Monitor set		
72	48		RO	Reserved Channel Monitor set		
73	49		RO	Reserved Channel Monitor set		
74	4A			Vendor Specific		
75	4B			Vendor Specific		
76	4C			Vendor Specific		
77	4D			Vendor Specific		
78	4E			Vendor Specific		
79	4F			Vendor Specific		
80	50			Vendor Specific		
81	51			Vendor Specific		
82	52			Reserved		
83	53			Reserved		
84	54			Reserved		
85	55			Reserved		
86	56	7 ~ 4		Reserved	Control	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3	RW	Tx4 Disable		00
		2	RW	Tx3 Disable		
		1	RW	Tx2 Disable		
		0	RW	Tx1 Disable		
87	57	7	RW	Rx4_Rate_select MSB		00
		6	RW	Rx4_Rate_select LSB		
		5	RW	Rx3_Rate_select MSB		
		4	RW	Rx3_Rate_select LSB		
		3	RW	Rx2_Rate_select MSB		
		2	RW	Rx2_Rate_select LSB		
		1	RW	Rx1_Rate_select MSB		
		0	RW	Rx1_Rate_select LSB		
88	58	7	RW	Tx4_Rate_select MSB		00
		6	RW	Tx4_Rate_select LSB		
		5	RW	Tx3_Rate_select MSB		
		4	RW	Tx3_Rate_select LSB		
		3	RW	Tx2_Rate_select MSB		
		2	RW	Tx2_Rate_select LSB		
		1	RW	Tx1_Rate_select MSB		
		0	RW	Tx1_Rate_select LSB		
89	59		RW	Software Application Select per SFF-8079, Rx Channel 4		00
90	5A		RW	Software Application Select per SFF-8079, Rx Channel 3		00
91	5B		RW	Software Application Select per SFF-8079, Rx Channel 2		00
92	5C		RW	Software Application Select per SFF-8079, Rx Channel 1		00
93	5D	7 ~ 3		Reserved		00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		2	RW	High Power Class Enable (Classes 5-7). When set (= 1b) enables Power Classes 5 to 7 in Byte 129 to exceed 3.5W. When cleared (= 0b), modules with Power classes 5 to 7 must dissipate less than 3.5W (but are not required to be fully functional). Default 0.		
		1	RW	Power set to Low Power Mode Default 0		
		0	RW	Override of LP mode signal setting the power mode with software		
94	5E		RW	Tx4_Application_Select		00
95	5F		RW	Tx3_Application_Select		00
96	60		RW	Tx2_Application_Select		00
97	61		RW	Tx1_Application_Select		00
98	62	7	RW	Tx4_CDR_control (1b = CDR on, 0b = CDR off)		Default FF
		6	RW	Tx3_CDR_control (1b = CDR on, 0b = CDR off)		
		5	RW	Tx2_CDR_control (1b = CDR on, 0b = CDR off)		
		4	RW	Tx1_CDR_control (1b = CDR on, 0b = CDR off)		
		3	RW	Rx4_CDR_control (1b = CDR on, 0b = CDR off)		
		2	RW	Rx3_CDR_control (1b = CDR on, 0b = CDR off)		
		1	RW	Rx2_CDR_control (1b = CDR on, 0b = CDR off)		
		0	RW	Rx1_CDR_control (1b = CDR on, 0b = CDR off)		
99	63			Reserved		00
100	64	7	RW	Masking bit Tx4 LOS		Default 00
		6	RW	Masking bit-Tx3 LOS		
		5	RW	Masking bit-Tx2 LOS		
		4	RW	Masking bit-Tx1 LOS		
		3	RW	Masking bit-Rx4 LOS		
		2	RW	Masking bit-Rx3 LOS		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1	RW	Masking bit-Rx2 LOS		
		0	RW	Masking bit-Rx1 LOS		
101	65	7	RW	Masking bit Tx4 Adapt EQ Fault		Default 00
		6	RW	Masking bit Tx3 Adapt EQ Fault		
		5	RW	Masking bit Tx2 Adapt EQ Fault		
		4	RW	Masking bit Tx1 Adapt EQ Fault		
		3	RW	Masking bit Tx4 Transmitter Fault		
		2	RW	Masking bit Tx3 Transmitter Fault		
		1	RW	Masking bit Tx2 Transmitter Fault		
		0	RW	Masking bit Tx1 Transmitter Fault		
102	66	7	RW	Masking bit -Tx4 CDR LOL		Default 00
		6	RW	Masking bit -Tx3 CDR LOL		
		5	RW	Masking bit -Tx2 CDR LOL		
		4	RW	Masking bit -Tx1 CDR LOL		
		3	RW	Masking bit -Rx4 CDR LOL		
		2	RW	Masking bit -Rx3 CDR LOL		
		1	RW	Masking bit -Rx2 CDR LOL		
		0	RW	Masking bit -Rx1 CDR LOL		
103	67	7	RW	Masking Bit for high Temperature alarm		Default 00
		6	RW	Masking Bit for low Temperature alarm		
		5	RW	Masking Bit for high Temperature warning		
		4	RW	Masking Bit for low Temperature warning		
		3 ~ 0	RW	Reserved		
104	68	7	RW	Masking Bit for high Vcc alarm		Default 00
		6	RW	Masking Bit for low Vcc alarm		
		5	RW	Masking Bit for high Vcc warning		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4	RW	Masking Bit for low Vcc warning		
		3 ~ 0	RW	Reserved		
105	69			Vendor Specific		00
106	6A			Vendor Specific		00
107	6B		RW	Reserved		00
108	6C		RO	Most significant byte of propagation delay		00
109	6D		RO	Least significant byte of propagation delay		00
110	6E	7 ~ 4	RO	Advanced Low Power Mode		00
		3	RO	Far Side Managed: A value of 1 indicates that the far end is managed and complies with SFF-8636.		
		2 ~ 0	RO	Min Operating Voltage		
111	6F			Assigned for use by PCI Express		00
112	70			Assigned for use by PCI Express		00
113	71	7		Reserved		00
		6 ~ 4	RO	=000 Far end is unspecified =001 Cable with single far end with 4 channels implemented, or separable module with 4-channel connector =010 Cable with single far end with 2 channels implemented, or separable module with 2-channel connector =011 Cable with single far end with 1 channel implemented, or separable module with 1-channel connector =100 4 far ends with 1 channel implemented in each (i.e. 4x1 break out) =101 2 far ends with 2 channels implemented in each (i.e. 2x2 break out) =110 2 far ends with 1 channel implemented in each (i.e. 2x1 break out)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3 ~ 0	RO	Near End Implementation: Bit 0 =0 Channel 1 implemented =1 Channel 1 not implemented Bit 1 =0 Channel 2 implemented =1 Channel 2 not implemented Bit 2 =0 Channel 3 implemented =1 Channel 3 not implemented Bit 3 =0 Channel 4 implemented =1 Channel 4 not implemented		
114	72		RW	Reserved	DataPathInit_MaxDuration for microQSFP. 0000b=Not Implemented.	00
115	73		RW	Reserved	Reserved	00
116	74		RW	Reserved	Reserved	00
117	75		RW	Password change area	Reserved	00
118	76		RW	Password change area	Reserved	00
119	77		WO	Password change area	Reserved	
120	78		WO	Password change area	Reserved	
121	79		WO	Password change area	Reserved	
122	7A		WO	Password change area	Reserved	
123	7B		WO	Password Entry area	Reserved	
124	7C		WO	Password Entry area	Reserved	
125	7D		WO	Password Entry area	Reserved	
126	7E		WO	Password Entry area	Reserved	
127	7F		WO	Page Select Byte		

ADDRESS A0H UPPER PAGE 00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
128	80		RO	Identifier	QSFP28 (SFF-8665)	11
129	81	7 ~ 6	RO	Extended Identifier		CC
				00: Power Class 1 (1.5 W max)	Power Class 4 (3.5 W max)	
				01: Power Class 2 (2.0 W max)		
				10: Power Class 3 (2.5 W max)		
				11: Power Class 4 (3.5 W max)		
		5		Reserved		
		4		0: No CLEI code present in Page 02h	No CLEI code present in Page 02h	
				1: CLEI code present in Page 02h		
		3		0: No CDR in TX , 1: CDR present in TX	CDR present in Tx	
		2		0: No CDR in RX , 1: CDR present in RX	CDR present in Rx	
		1 ~ 0		00: unused (legacy setting)	Unused	
				01: Power Class 5 (4.0 W max) See Byte 93 bit 2 to enable		
				10: Power Class 6 (4.5 W max) See Byte 93 bit 2 to enable		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
				11: Power Class 7 (5.0 W max) See Byte 93 bit 2 to enable		
130	82		RO	Connector Type	LC	07
131	83	7	RO	The Extended Specification Compliance: Codes are maintained in the Transceiver Management section of SFF-8024. See byte 192	TRUE	80
		6		10GBASE-LRM	FALSE	
		5		10GBASE-LR	FALSE	
		4		10GBASE-SR	FALSE	
		3		40GBASE-CR4	FALSE	
		2		40GBASE-SR4	FALSE	
		1		40GBASE-LR4	FALSE	
		0		40G Active Cable (XLPPI)	FALSE	
132	84	7 ~ 3		Reserved		00
		2		OC 48, long reach	FALSE	
		1		OC 48, intermediate reach	FALSE	
		0		OC 48 short reach	FALSE	
133	85	7		Reserved SAS		00
		6		SAS 12.0 Gbps	FALSE	
		5		SAS 6.0 Gbps	FALSE	
		4		SAS 3.0 Gbps	FALSE	
		3 ~ 0		Reserved		
134	86	7 ~ 4		Reserved		00
		3		1000BASE-T	FALSE	
		2		1000BASE-CX	FALSE	
		1		1000BASE-LX	FALSE	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		0		1000BASE-SX	FALSE	
135	87	7		Very long distance (V)	FALSE	00
		6		Short distance (S)	FALSE	
		5		Intermediate distance (I)	FALSE	
		4		Long distance (L)	FALSE	
		3		Medium (M)	FALSE	
		2		Reserved		
		1		Longwave laser (LC)	FALSE	
		0		Electrical inter-enclosure (EL)	FALSE	
136	88	7		Electrical intra-enclosure	FALSE	00
		6		Shortwave laser w/o OFC (SN)	FALSE	
		5		Shortwave laser w OFC (SL)	FALSE	
		4		Longwave Laser (LL)	FALSE	
		3 ~0		Reserved		
137	89	7	RO	Twin Axial Pair (TW)	FALSE	00
		6		Shielded Twisted Pair (TP)	FALSE	
		5		Miniature Coax (MI)	FALSE	
		4		Video Coax (TV)	FALSE	
		3		Multi-mode 62.5 m (M6)	FALSE	
		2		Multi-mode 50 m (M5)	FALSE	
		1		Multi-mode 50 um (OM3)	FALSE	
		0		Single Mode (SM)	FALSE	
138	8A	7	RO	1200 MBytes/Sec	FALSE	00
		6		800 MBytes/Sec	FALSE	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		5		1600 MBytes/Sec	FALSE	
		4		400 MBytes/Sec	FALSE	
		3		3200 MBytes/sec	FALSE	
		2		200 MBytes/Sec	FALSE	
		1		Extended see Byte 192	FALSE	
		0		100 Mbytes/Sec	FALSE	
139	8B			Encoding	256B/257B	07
140	8C			Nominal bit rate, units of 100 Mbps.	255	FF
141	8D	7 ~ 2	RO	Reserved		00
		1		QSFP+ Rate Select Version 2	FALSE	
		0		QSFP+ Rate Select Version 1	FALSE	
142	8E		RO	Link length supported for SMF fiber in km	0	00
143	8F		RO	Link length supported for EBW 50/125 um fiber (OM3), units of 2 m	38(75 m)	26
144	90		RO	Link length supported for 50/125 um fiber (OM2), units of 1 m	0	00
145	91		RO	Link length supported for 62.5/125 um fiber (OM1), units of 1 m	0	00
146	92		RO	Link length supported for EBW 50/125 um fiber (OM4), units of 2 m	50(100 m)	32
147	93	7 ~ 4	RO	Transmitter Technology	850 nm VCSEL	00
		3		0: No Wavelength Control ; 1: Active Wavelength Control	FALSE	
		2		0: Uncooled transmitter device; 1: Cooled transmitter	FALSE	
		1		0: Pin detector; 1: APD detector	FALSE	
		0		0: Transmitter not Tunable ; 1: Transmitter Tunable	FALSE	
148	94		RO	Vendor Name	F	46
149	95				I	49
150	96				N	4E

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
151	97				I	49
152	98				S	53
153	99				A	41
154	9A				R	52
155	9B					20
156	9C				C	43
157	9D				O	4F
158	9E				R	52
159	9F				P	50
160	A0					20
161	A1					20
162	A2					20
163	A3					20
164	A4	7 ~ 5	RO	Reserved		00
		4		EDR (20.0 Gb/s)	FALSE	
		3		FDR (14.0 Gb/s)	FALSE	
		2		QDR (10.0 Gb/s)	FALSE	
		1		DDR (5.0 Gb/s)	FALSE	
		0		SDR (2.5 Gb/s)	FALSE	
165	A5		RO	Vendor OUI: IEEE Company ID	00 90 65h (36965 Decimal)	00
166	A6					90
167	A7					65
168	A8		RO	Vendor Part Number	F	46
169	A9				T	54
170	AA				L	4C
171	AB				C	43

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
172	AC				9	39
173	AD				1	31
174	AE				5	35
175	AF				2	32
176	B0				R	52
177	B1				G	47
178	B2				P	50
179	B3				L	4C
180	B4					20
181	B5					20
182	B6					20
183	B7					20
184	B8		RO	Vendor Revision	A0	41
185	B9					30
186	BA		RO	Wavelength. (Wavelength = Value/20 in nm)	850 nm	42
187	BB					68
188	BC		RO	Wavelength tolerance. (Wavelength Tol.= value/200 in nm)	1400(7 nm)	05
189	BD					78
190	BE		RO	Maximum Case Temperature. If 70 deg C then use 0	70 °C	00
191	BF		RO	Check code for base ID fields (bytes 128-190)		DE
192	C0		RO	Link Codes: Extended Specification Compliance Codes	100G SWDM4	20
193	C1	7 ~ 5	RO	Reserved		07
		4		Tx Input Adaptive Equalization Freeze Capable	not implemented	
		3		TX Input Equalization Auto Adaptive Capable, coded 1 if implemented, else 0.	not implemented	
		2		TX Input Equalization Fixed Programmable Settings, coded 1 if implemented, else 0	implemented	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1		RX Output Emphasis Fixed Programmable Settings, coded 1 if implemented, else 0.	implemented	
		0		RX Output Amplitude Fixed Programmable Settings, coded 1 if implemented, else 0.	implemented	
194	C2	7	RO	TX CDR On/Off Control implemented, (1b if controllable, 0b if fixed).	implemented	FF
		6		RX CDR On/Off Control implemented, (1b if controllable, 0b if fixed)	implemented	
		5		Tx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	implemented	
		4		Rx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	implemented	
		3		Rx Squelch Disable implemented, coded 1 if implemented, else 0	implemented	
		2		Rx Output Disable capable: coded 1 if implemented, else 0.	implemented	
		1		Tx Squelch Disable implemented: coded 1 if implemented, else 0	implemented	
		0		Tx Squelch implemented: coded 1 if implemented, else 0	implemented	
195	C3	7	RO	Memory page 02 provided: coded 1 if implemented, else 0	implemented	D6
		6		Memory Page 01h provided: coded 1 if implemented, else 0	implemented	
		5		RATE_SELECT, 1 if implemented, else 0	not implemented	
		4		Tx_DISABLE is implemented and disables the serial output	implemented	
		3		Tx_FAULT signal implemented, coded 1 if implemented, else 0	not implemented	
		2		Tx Squelch implemented to reduce OMA coded 0, implemented to reduce Pave coded 1.	implemented	
		1		Tx Loss of Signal implemented, coded 1 if implemented, else 0	implemented	
		0		Memory Pages 20h & 21h Implemented.	not implemented	
196	C4		RO	Vendor Serial Number	Vendor Serial Number (ASCII)	xx
197	C5					xx
198	C6					xx
199	C7					xx
200	C8					xx
201	C9					xx
202	CA					xx

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
203	CB					xx
204	CC					xx
205	CD					xx
206	CE					xx
207	CF					xx
208	D0					xx
209	D1					xx
210	D2					xx
211	D3					xx
212	D4		RO	Date Code	ASCII code, two low order digits of year. (00=2000).	xx
213	D5					xx
214	D6				ASCII code, digits of month (01=Jan through 12=Dec)	xx
215	D7					xx
216	D8				ASCII code, day of month (01-31)	xx
217	D9					xx
218	DA				ASCII code, vendor specific lot code, may be blank	xx
219	DB					xx
220	DC	7 ~ 6	RO	Reserved		3C
		5		Temperature monitoring implemented	TRUE	
		4		Supply voltage monitoring implemented	TRUE	
		3		Received power measurements type. 0=OMA 1=Average Power	Average power	
		2		Transmitter power measurement. 0=Not supported 1=Supported	TRUE	
		1 ~ 0		Reserved		
221	DD	7 ~ 5	RO	Reserved		10

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4		Initialization Complete Flag implemented. This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at byte 6, bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module	Implemented	
		3		Rate Selection Declaration: When this Declaration bit is 0 the free side device does not support rate selection. When this Declaration bit is 1, rate selection is implemented using extended rate selection.	FALSE	
		2		Application Select Table Declaration: When this Declaration bit is 1, the free side device supports rate selection using application select table mechanism. When this Declaration bit is 0, the free side device does not support application select and Page 01h does not exist	FALSE	
		1		TC readiness flag implemented	FALSE	
		0		Reserved		
222	DE		RO	BR Nominal, units of 250 Mbps. Complements Byte 140.	103(25.75 Gbps)	67
223	DF		RO	Check code for the Extended ID Fields (bytes 192-222)		
224	E0		RO	Vendor Specific EEPROM		00
225	E1					00
226	E2					00
227	E3					00
228	E4					00
229	E5					00
230	E6					00
231	E7					00
232	E8					00
233	E9					00
234	EA					00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
235	EB					00
236	EC					00
237	ED					00
238	EE					00
239	EF					00
240	F0					00
241	F1					00
242	F2					00
243	F3					00
244	F4					00
245	F5					00
246	F6					00
247	F7					00
248	F8					00
249	F9					00
250	FA					00
251	FB					00
252	FC					00
253	FD					00
254	FE					00
255	FF					00

ADDRESS A0H PAGE 01 APPLICATION SELECT

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value

128	80		RO	CC_APPS:	Check code for the AST: the check code shall be the low order bits of the sum of the contents of all the bytes from byte 129 to byte 255, inclusive.	00
129	81	7 ~ 6	RO	Reserved		00
		5 ~ 0		AST Table Length, TL (length - 1):	A 6 bit binary number. TL, specifies the offset of the last application table entry defined in bytes 130-255. TL is valid between 0 (1 entry) and 62 (for a total of 63 entries)	
130	82		RO	Application Code 0	Definition of first application supported	00 00
131	83					
132 ~ 255	84 ~ FF		RO	Application Code TL		

ADDRESS A0H PAGE 02 USER WRITABLE EEPROM

Byte Addr	Hex	LSB	Name	Description	Hex Value
128	80		User EEPROM Data	Customer CLEI code, if page 00h byte 129 is set	
129 ~ 255	81 ~ FF		User EEPROM Data	User EEPROM Data Initialization	

ADDRESS A0H PAGE 03

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
128	80		RO	Temperature High Alarm Threshold MSB	75 °C	4B
129	81			Temperature High Alarm Threshold LSB		00
130	82		RO	Temperature Low Alarm Threshold MSB	-5 °C	FB
131	83			Temperature Low Alarm Threshold LSB		00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
132	84		RO	Temperature High Warning Threshold MSB	70 °C	46
133	85			Temperature High Warning Threshold LSB		00
134	86		RO	Temperature Low Warning Threshold MSB	0 °C	00
135	87			Temperature Low Warning Threshold LSB		00
136	88			Reserved		
137	89			Reserved		
138	8A			Reserved		
139	8B			Reserved		
140	8C			Reserved		
141	8D			Reserved		
142	8E			Reserved		
143	8F			Reserved		
144	90		RO	Vcc High Alarm Threshold MSB	3.63 V	8D
145	91			Vcc High Alarm Threshold LSB		CC
146	92		RO	Vcc Low Alarm Threshold MSB	2.97 V	74
147	93			Vcc Low Alarm Threshold LSB		04
148	94		RO	Vcc High Warning Threshold MSB	3.465 V	87
149	95			Vcc High Warning Threshold LSB		5A
150	96		RO	Vcc Low Warning Threshold MSB	3.135 V	7A
151	97			Vcc Low Warning Threshold LSB		76
152	98			Reserved		
153	99			Reserved		
154	9A			Reserved		
155	9B			Reserved		
156	9C			Reserved		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
157	9D			Reserved		
158	9E			Reserved		
159	9F			Reserved		
160	A0			Vendor Specific		
161	A1			Vendor Specific		
162	A2			Vendor Specific		
163	A3			Vendor Specific		
164	A4			Vendor Specific		
165	A5			Vendor Specific		
166	A6			Vendor Specific		
167	A7			Vendor Specific		
168	A8			Vendor Specific		
169	A9			Vendor Specific		
170	AA			Vendor Specific		
171	AB			Vendor Specific		
172	AC			Vendor Specific		
173	AD			Vendor Specific		
174	AE			Vendor Specific		
175	AF			Vendor Specific		
176	B0		RO	Rx Power High Alarm Threshold MSB	5.5 dBm	8A
177	B1			Rx Power High Alarm Threshold LSB		99
178	B2		RO	Rx Power Low Alarm Threshold MSB	-16.0 dBm	00
179	B3			Rx Power Low Alarm Threshold LSB		FB
180	B4		RO	Rx Power High Warning Threshold MSB	+4.5 dBm	6E
181	B5			Rx Power High Warning Threshold LSB		18
182	B6		RO	Rx Power Low Warning Threshold MSB	-13.0 dBm	01
183	B7			Rx Power Low Warning Threshold LSB		F5

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
184	B8		RO	Tx Bias Current High Alarm Threshold MSB	11 mA	15
185	B9			Tx Bias Current High Alarm Threshold LSB		7C
186	BA		RO	Tx Bias Current Low Alarm Threshold MSB	2 mA	03
187	BB			Tx Bias Current Low Alarm Threshold LSB		E8
188	BC		RO	Tx Bias Current High Warning Threshold MSB	10 mA	13
189	BD			Tx Bias Current High Warning Threshold LSB		88
190	BE		RO	Tx Bias Current Low Warning Threshold MSB	3 mA	05
191	BF			Tx Bias Current Low Warning Threshold LSB		DC
192	C0		RO	Tx Power High Alarm Threshold MSB	+6 dBm	9B
193	C1			Tx Power High Alarm Threshold LSB		83
194	C2		RO	Tx Power Low Alarm Threshold MSB	-7 dBm	07
195	C3			Tx Power Low Alarm Threshold LSB		CB
196	C4		RO	Tx Power High Warning Threshold MSB	+5 dBm	7B
197	C5			Tx Power High Warning Threshold LSB		87
198	C6		RO	Tx Power Low Warning Threshold MSB	-6 dBm	09
199	C7			Tx Power Low Warning Threshold LSB		D0
200	C8			Reserved		
201	C9			Reserved		
202	CA			Reserved		
203	CB			Reserved		
204	CC			Reserved		
205	CD			Reserved		
206	CE			Reserved		
207	CF			Reserved		
208	D0			Vendor Specific		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
209	D1			Vendor Specific		
210	D2			Vendor Specific		
211	D3			Vendor Specific		
212	D4			Vendor Specific		
213	D5			Vendor Specific		
214	D6			Vendor Specific		
215	D7			Vendor Specific		
216	D8			Vendor Specific		
217	D9			Vendor Specific		
218	DA			Vendor Specific		
219	DB			Vendor Specific		
220	DC			Vendor Specific		
221	DD			Vendor Specific		
222	DE			Vendor Specific		
223	DF			Vendor Specific		
224	E0	7 ~ 4	RO	Max TX input equalization	10 dB (please refer to Table1 pg 33)	A7
		3 ~ 0		Max RX output emphasis	7 dB (please refer to Table 2 pg 34)	
225	E1	7 ~ 6	RO	Reserved		0F
		5 ~ 4		Rx output emphasis type: '=00 Peak-to-peak amplitude stays constant, or not implemented =01 Steady state amplitude stays constant =10 Average of peak-to-peak and steady state amplitudes stays constant =11 Reserved	Peak-to-peak amplitude stays constant, or not implemented	
		3		RX output amplitude support: Amplitude code 0011 (600-1200 mV P-P)	supported	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		2		RX output amplitude support: Amplitude code 0010 (400-800 mV P-P)	supported	
		1		RX output amplitude support: Amplitude code 0001 (300-600 mV P-P)	supported	
		0		RX output amplitude support: Amplitude code 0000 (100-400 mV P-P)	supported	
226	E2			Reserved		00
227	E3			Reserved		00
228	E4		RO	Max TC stabilization time, units of 1 s		00
229	E5		RO	Max CTLE Adaptive Algorithm setting time, units of 100 ms		00
230	E6			Reserved		
231	E7			Reserved		
232	E8			Reserved		
233	E9	4-7		Reserved		00
		3		TX1 Adaptive Equalization Freeze	FALSE	
		2		TX2 Adaptive Equalization Freeze	FALSE	
		1		TX3 Adaptive Equalization Freeze	FALSE	
		0	RO	TX4 Adaptive Equalization Freeze	FALSE	
234	EA	7 ~ 4	RW	TX1 input equalization control	(please refer to Table 1 pg 33)	00
		3 ~ 0	RW	TX2 input equalization control		
235	EB	7 ~ 4	RW	TX3 input equalization control		00
		3 ~ 0	RW	TX4 input equalization control		
236	EC	7 ~ 4	RW	RX1 output emphasis control	(please refer to Table 2 pg 34)	00
		3 ~ 0	RW	RX2 output emphasis control		
237	ED	7 ~ 4	RW	RX3 output emphasis control		00
		3 ~ 0	RW	RX4 output emphasis control		
238	EE	7 ~ 4	RW	RX1 output amplitude control	(please refer to Table 3 pg 35)	22

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3 ~ 0	RW	RX2 output amplitude control		
239	EF	7 ~ 4	RW	RX3 output amplitude control		22
		3 ~ 0	RW	RX4 output amplitude control		
240	F0	7	RW	Rx Squelch Disable Channel 4	FALSE	00
		6	RW	Rx Squelch Disable Channel 3	FALSE	
		5	RW	Rx Squelch Disable Channel 2	FALSE	
		4	RW	Rx Squelch Disable Channel 1	FALSE	
		3	RW	Tx Squelch Disable Channel 4	FALSE	
		2	RW	Tx Squelch Disable Channel 3	FALSE	
		1	RW	Tx Squelch Disable Channel 2	FALSE	
		0	RW	Tx Squelch Disable Channel 1	FALSE	
241	F1	7	RW	Rx Output Disable channel 4	FALSE	00
		6	RW	Rx Output Disable channel 3	FALSE	
		5	RW	Rx Output Disable channel 2	FALSE	
		4	RW	Rx Output Disable channel 1	FALSE	
		3	RW	TX4 adaptive equalization control	Not implemented	
		2	RW	TX3 adaptive equalization control	Not implemented	
		1	RW	TX2 adaptive equalization control	Not implemented	
		0	RW	TX1 adaptive equalization control	Not implemented	
242	F2	7	RW	Masking Bit for high RX Power alarm Channel 1		00
		6	RW	Masking Bit for low RX Power alarm Channel 1		
		5	RW	Masking Bit for high RX Power warning channel 1		
		4	RW	Masking Bit for low RX Power warning channel 1		
		3	RW	Masking Bit for high RX Power alarm channel 2		
		2	RW	Masking Bit for low RX Power alarm channel 2		
		1	RW	Masking Bit for high RX Power warning channel 2		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		0	RW	Masking Bit for low RX Power warning channel 2		
243	F3	7	RW	Masking Bit for high RX Power alarm channel 3		00
		6	RW	Masking Bit for low RX Power alarm channel 3		
		5	RW	Masking Bit for high RX Power warning channel 3		
		4	RW	Masking Bit for low RX Power warning channel 3		
		3	RW	Masking Bit for high RX Power alarm channel 4		
		2	RW	Masking Bit for low RX Power alarm channel 4		
		1	RW	Masking Bit for high RX Power warning channel 4		
		0	RW	Masking Bit for low RX Power warning channel 4		
244	F4	7	RW	Masking Bit for high TX Bias alarm channel 1		00
		6	RW	Masking Bit for low TX Bias alarm channel 1		
		5	RW	Masking Bit for high TX Bias warning channel 1		
		4	RW	Masking Bit for low TX Bias warning channel 1		
		3	RW	Masking Bit for low TX Bias warning channel 1		
		2	RW	Masking Bit for low TX Bias alarm channel 2		
		1	RW	Masking Bit for high TX Bias warning channel 2		
		0	RW	Masking Bit for low TX Bias warning channel 2		
245	F5	7	RW	Masking Bit for high TX Bias alarm channel 3		00
		6	RW	Masking Bit for low TX Bias alarm channel 3		
		5	RW	Masking Bit for high TX Bias warning channel 3		
		4	RW	Masking Bit for low TX Bias warning channel 3		
		3	RW	Masking Bit for high TX Bias alarm channel 4		
		2	RW	Masking Bit for low TX Bias alarm channel 4		
		1	RW	Masking Bit for high TX Bias warning channel 4		
		0	RW	Masking Bit for low TX Bias warning channel 4		
246	F6	7	RW	Masking Bit for high TX Power alarm channel 1		00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		6	RW	Masking Bit for low TX Power alarm channel 1		
		5	RW	Masking Bit for high TX Power warning channel 1		
		4	RW	Masking Bit for low TX Power warning channel 1		
		3	RW	Masking Bit for high TX Power alarm channel 2		
		2	RW	Masking Bit for low TX Power alarm channel 2		
		1	RW	Masking Bit for high TX Power warning channel 2		
		0	RW	Masking Bit for low TX Power warning channel 2		
247	F7	7	RW	Masking Bit for high TX Power alarm channel 3		00
		6	RW	Masking Bit for low TX Power alarm channel 3		
		5	RW	Masking Bit for high TX Power warning channel 3		
		4	RW	Masking Bit for low TX Power warning channel 3		
		3	RW	Masking Bit for high TX Power alarm channel 4		
		2	RW	Masking Bit for low TX Power alarm channel 4		
		1	RW	Masking Bit for high TX Power warning channel 4		
		0	RW	Masking Bit for low TX Power warning channel 4		
248			RW	Reserved channel monitor masks set 4		00
249			RW	Reserved channel monitor masks set 4		00
250			RW	Reserved		
251			RW	Reserved		
252			RW	Reserved		
253			RW	Reserved		
254			RW	Reserved		
255			RW	Reserved		

CTLE CHARACTERIZATION TABLE 1

We have characterized the CTLE for QSFP28 SWDM and the following table lists our results.
We can set the default CTLE per host recommendation. Please note that the current implement for CTLE is fixed programmable and not adaptive. Current default setting for bytes 234 and 235 is 0x00.

MSA Byte 234 & 235	Overall EQ CTLE peaking (dB) Need values for SWDM
0	**0**
1	1.4
2	2.4
3	3.3
4	4.6
5	5.8
6	6.6
7	7.6
8	8.2
9	8.7
A	8.7
B	8.7
C	8.7
D	8.7
E	8.7

Rx EMPHASIS CONTROL TABLE 2

We can set the default Rx Emphasis per host recommendation. Current default is 0x00

Total EQ peaking (dB) Need values for SWDM	MSA Register 236 & 237
1.3	**0**
2	1
2.3	2
3	3
3.8	4
4.6	5
5.6	6
6.6	7
7.4	8
8.1	9
8.9	A
9.7	B
10.6	C
11.6	D
12.4	E
13.4	F

Rx OUTPUT DIFFERENTIAL AMPLITUDE CONTROL TABLE 3

Code	Receiver Output Amplitude (No Output Equalization)	
	Nominal	Units
1xxx	Reserved	mV (p-p)
0111	Reserved	mV (p-p)
0110	Reserved	mV (p-p)
0101	Reserved	mV (p-p)
0100	Reserved	mV (p-p)
0011	600 - 1200	mV (p-p)
0010 (Default)	**400 - 800**	**mV (p-p)**
0001	300 - 600	mV (p-p)
0000	100 - 400	mV (p-p)

*Default setting for the Rx output amplitude is 0010 (400 – 800mV p-p). This corresponds to MSA Range 2

Recommended Initialization for QSFP28 SWDM transceivers

1. Host board is powered on and initialized. The QSFP28 module may or may not already be plugged into the host board. Host should implement low power mode (LPMode pin 31, active High) and hold the module in reset (RESETL pin 9 active low)

2. The host PHY is enabled and configured to the settings that meet the host compliance point TP1.

3. Host brings up the MAC/PCS interface, and CAUI-4 idle packets are transmitted.

4. If not already present in step 1, the QSFP28 module is hot plugged into host.

5. The host releases RESET, and allows 2 seconds for the module to be ready to communicate over the I2C.

6. QSFP28 module is held in Tx disable state by setting Byte 86 to value 0x0F

7. The module ID EEPROM is read and the host configures to the appropriate settings. Host can re-configure the CTLE setting if required.

8. The host releases LPMode pin and releases Tx Disable, the module goes to high power state.

9. Once the optical connections are implemented, the host physical layer link indicator should be asserted.

10. The host will need to read Page 0 byte 2 to clear the latched interrupt state. Page 0 Byte 2 reflects the digital state of the Interrupt pin 28.
    The host should clear the latched Interrupt state by first readings all alarm and warning flags along with the Initialization complete flag in Page 0 Byte 6.
    Once the latched Interrupt state has cleared then the Interrupt pin 28 (IntL) will go to high logic state.

11. The MAC/PCS interface can start transmitting data.

Finisar Contact Information

Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089-1134
(408) 548-1000
www.finisar.com
sales@finisar.com